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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,170	11/26/2003	Matthew Brady Henson	SIG000117	5742

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EXAMINER	
PAUL, DISLER	
ART UNIT	PAPER NUMBER
2615	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,170	HENSON ET AL.	
	Examiner	Art Unit	
	Disler Paul	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al."US 6,759,906 B2") and Aubauer et al.("US 2005/0276423 A1").

Re claim 1, Matsunaga et al. discloses a microphone bias circuit for use within an integrated circuit having a microphone input ("*fig.26-is the whole integrated circuit of microphone input(323)*"), the microphone bias circuit comprises: a first integrated circuit (IC) pin ("*fig.1- is a detail description of the first integrated circuit & col.8 line 49-54*"); a first resistor operably coupled to the first IC pin("*fig.1/R1*") and a return voltage ("fig.1/(vg1) gate bias voltage"); a second IC pin operably coupled to receive analog signals from a microphone("*fig.6/(#71-85)-is the second IC pin which receive analog signal from(80) & fig.26-with microphone(323)*"); and a supply voltage buffer operably coupled to produce a buffered supply voltage based on a impedance setting ("*fig.7/(#AMP1,R11)*"), wherein at least one off-chip component couples the second IC pin to the first IC pin("*fig.5-(Pout,Vapc)couple the two IC pins*")and wherein the supply

voltage buffer provides the buffered supply voltage to second IC pin as a microphone bias voltage("*fig.6,fig.7-buffer volt(70) is provided to ic circuit(vg1,vg2) as bias*"). Matsunaga et al. fail to disclose the supply voltage as being variable based on variable impedance. However, Aubauer et al. disclose of a microphone arrangement in order to process audio signal in which having variable supply voltage based on variable impedance("fig.7 & page 2[0053] line 7-12") for purpose of minimizing circuit complexity as well as cost being adapted for most applications.

Therefore taking the combined teaching of Matsunaga et al. and Aubauer et al. as a whole, one of the ordinary skill in the art would have found it obvious to incorporate variable supply voltage based on variable impedance in Matsunaga et al. for the purpose of minimizing circuit complexity as well as cost being adapted for most applications as taught by as taught by Aubauer et al.

Re claim 2, the microphone bias circuit of claim 1, wherein the power supply buffer comprises: an amplifier having a first input, a second input,and an output("*Matsunaga,fig.7/(AMP1)*"), wherein the first input is coupled to receive a bandgap voltage ("*Matsunaga,col.13 line 63-67 & fig.10/(11,112)*") and the output provides the buffered supply voltage("*Matsunaga,fig.11/buffer output(vo)*"); and a variable impedance("*Aubauer,fig.7/z1*") having a first node, a second node, and a tap node, wherein the first node is coupled to the output of the

amplifier, the second node is coupled to the return voltage, and the tap node is coupled to the second input of the amplifier("*Matsunaga,fig.11/node to (-vapc,vo,vdd)*").

Re claim 3, The microphone bias circuit of claim 2, wherein the variable impedance comprises an on-chip variable resistor circuit("*Aubauer,fig.7/zl*").

Re claim 4, The microphone bias circuit of claim 1, wherein the at least one off-chip component comprises a capacitor ("*Matsunaga,fig.1/(c1-c4); col.9 line 5-10*").

Re claim 5, the microphone bias circuit of claim 1 further comprises: a second resistor coupled between the variable supply voltage buffer and the second IC pin("*Matsunaga,fig.1/R2-is connected between the supply voltage and second pin-further info second pin see fig.6(71-85)*").

Re claim 6, the microphone bias circuit of claim 1 further comprises: a processing module("*Matsunaga,fig.26/351*"); and memory operably coupled to the processing module("*Matsunaga,fig.26/360,353*"), wherein the memory stores operational instructions that cause the processing module to: monitor the received analog signals("*Matsunaga,col.16 line 61-61-microprocessor(353) so as to provide control*; determining ("Aubauer,*fig.7 & page 1[0004] line 3-4*") whether the received analog signals are optimally biased ("*Matsunaga,fig.26/(323),biasing ciruit (fig.6)*"); and when the

received analog signals are not optimally biased, adjust the variable supply voltage buffer to optimally bias the received analog signals("*fig.7 & page 2[0053] line 7-12*").

Re claim 8, an integrated circuit for use in a multiple function handheld device("*fig.26,col.1 line 20*"), the integrated circuit comprises: a processing module operably coupled to perform at least one algorithm relating to a function of the multiple function handheld device("*fig.26/multifunction(330,340) to(351)*"); an analog to digital converter operably coupled to convert analog signals into digital signals ("*fig.6/81*"), wherein the digital signals are processed by the processing module while performing the at least one algorithm("*fig.26/351*"); a microphone input circuit("*fig.26/323,fig.1*") operably coupled to provide the analog signals to the analog to digital converter, wherein the microphone input circuit includes: an amplifier operably coupled to amplify received input analog signals to produce the analog signals("*fig.7/(AMP1,AMP2)*"); and a microphone bias circuit that includes: a first integrated circuit (IC) pin ("*fig.1- is a detailed descriptionof the formed first IC circuit & col.8 line 49-54*"); a first resistor operably coupled to the first IC pin("*fig.1/R1*") and a return voltage ("*fig.1/(vg1) gate bias voltage*"); a second IC pin operably coupled to receive analog signals from a microphone("*fig.6/(#71-85)- is the second IC pin which receive analog*

signal from(80) & fig.26-with microphone(323)"); and a supply voltage buffer operably coupled to produce a buffered supply voltage based on a impedance setting ("*fig.7/(#AMP1,R11)*"), wherein at least one off-chip component couples the second IC pin to the first IC pin("*fig.5-(Pout,Vapc)couple the two IC pins*")and wherein the supply voltage buffer provides the buffered supply voltage to second IC pin as a microphone bias voltage("*fig.6,fig.7-buffer volt(70) is provided to ic circuit(vg1,vg2) as bias*"). Matsunaga et al. fail to disclose the supply voltage as being variable based on variable impedance. However, Aubauer et al. disclose of a microphone arrangement in order to process audio signal in which having variable supply voltage based on variable impedance("fig.7 & page 2[0053] line 7-12") for purpose of minimizing circuit complexity as well as cost being adapted for most applications.

Therefore taking the combined teaching of Matsunaga et al. and Aubauer et al. as a whole, one of the ordinary skill in the art would have found it obvious to incorporate variable supply voltage based on variable impedance in Matsunaga et al. for the purpose of minimizing circuit complexity as well as cost being adapted for most applications as taught by as taught by Aubauer et al.

3. Claims 7, 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al."US 6,759,906 B2") and Aubauer et al.("US 2005/0276423 A1") as applied to claims 1 and 8 above, and further in view of Melo et al.(US 6,243,817 B1").

Re claim 7, the combination of Matsunaga et al. and Aubauer et al. as a whole fails to disclose the buffer comprising a power down input operably coupled to receive a power down signal, wherein, when the power down signal is in a first state, the supply voltage buffer is enabled and when the power down signal is in a second state, the supply voltage buffer is disabled. However, Meto et al. disclose a computer having plurality input buffers which a power down input operably coupled to receive a power down signal, wherein, when the power down signal is in a first state, the supply voltage buffer is enabled and when the power down signal is in a second state, the supply voltage buffer is disabled("*col.3 line 18-26*") for the purpose of power management in conserving power.

Therefore taking the combined teaching of Matsunaga et al. and Aubauer et al. and Melo et al. as a whole, one of the ordinary skill in the art would have found it obvious to incorporate the input buffers which a power down input operably coupled to receive a power down signal, wherein, when the power down signal is in a first state, the supply voltage buffer is enabled and when the power down signal is in a second state, the supply voltage buffer is disabled for the purpose of power management in conserving power as taught by Melo et al.

Re claims 9-14 have been analyzed and rejected with respect to claim 2-7 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Disler Paul whose telephone number is 571-272-2222. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-2000. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DP

VU LE
SUPERVISORY PATENT EXAMINER